

**AMENDMENTS**

Please amend the above-referenced application as follows:

***IN THE CLAIMS:***

This listing of claims replaces all prior versions and listings of claims in the application.

1 1-23. (Canceled)

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1 24. (Currently Amended) A method for finding a predefined plurality of  
2 instructions, if available, that are ready to be executed and that reside in an instruction  
3 reordering mechanism of a processor that can launch execution of instructions out of  
4 order via a predefined number of instruction ports, comprising the steps of:  
5 (a) providing said instruction reordering mechanism having a plurality of  
6 said instructions, each said instruction having a respective logic element for causing and  
7 preventing launching, when appropriate, of said instruction; and  
8 (b) propagating a set of signals successively through said logic elements of  
9 said instruction reordering mechanism, said set of signals responsive to available  
10 instruction ports and port information, wherein an instruction identified as valid for  
11 launching is launched on a select instruction port identified via propagation logic  
12 forwarded through said logic elements and wherein said propagation logic includes a next  
13 available instruction port identifier when an instruction port is available.

1 25. (Previously Presented) The method of claim 24, further comprising the  
2 step of:  
3 advising each instruction port of said instruction reordering mechanism during  
4 each launch cycle either that said instruction will be launched or that said instruction will  
5 not be launched.

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1           26.     (Previously Presented) The method of claim 24, wherein said signals are  
2 propagated through said logic elements only in response to logic transitions from a first  
3 logic level to a second logic level.

1           27.     (Previously Presented) The method of claim 24, further comprising the  
2 step of:  
3           communicating said predefined plurality of said instructions to a corresponding  
4 predefined plurality of instruction ports associated with one or more execution resources.

1           28.     (Previously Presented) The method of claim 24, further comprising the  
2 step of, after said predefined plurality of said instructions have been selected, propagating  
3 a lost signal to remaining logic elements associated with remaining instructions of said  
4 instruction reordering mechanism to indicate to said remaining logic elements that their  
5 respective remaining instructions have not been selected.

1           29.     (Previously Presented) The method of claim 24, further comprising the  
2 steps of:

3           (c)     after said predefined plurality of said instructions have been selected,  
4 propagating a lost signal to remaining logic elements associated with remaining  
5 instructions of said instruction reordering mechanism to indicate to said remaining logic  
6 elements that their respective remaining instructions have not been selected;

7           (d)     performing steps (b) and (c) during a single cycle associated with one or  
8 more execution resources; and

9           (e)     communicating said predefined plurality of said instructions from said  
10 instruction reordering mechanism to a corresponding predefined plurality of instruction  
11 ports associated with said one or more execution resources.

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1           30.   (Previously Presented) The method of claim 24, further comprising the  
2 step of:

3                   (c)   providing said instruction reordering mechanism in a form of a queue  
4 having a plurality of slots, each said slot having a respective one of said logic elements  
5 and means for temporarily storing a respective instruction; and

6                   (d)   propagating said set of said signals successively through said slots of said  
7 queue during an execution cycle.

1           31.   (Previously Presented) The method of claim 24, wherein said set comprises  
2 two or more signals.

1           32.   (Previously Presented) The method of claim 24, further comprising the  
2 step of:

3                   (c)   causing said propagation through only a predefined number of said logic  
4 elements during a launch cycle.

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1           33.     (Currently Amended) A method for quickly finding a predefined plurality  
2 of instructions, if available, that are ready to be executed and that reside in a queue of a  
3 processor that can launch the execution of instructions out of order, so that the found  
4 instructions can be communicated to a corresponding predefined plurality of ports  
5 associated with one or more execution resources, comprising the steps of:

6           (a)    providing said queue having a plurality of slots, each said slot for  
7 temporarily storing a respective instruction and launching, when appropriate, execution of  
8 said respective instruction; and

9           (b)    propagating a set of signals successively through slots of said queue  
10 during a launch cycle, said set of signals responsive to available instruction ports and port  
11 information to launch execution of an instruction that, when passed through a particular  
12 slot:

13               (1)   select said particular slot for launching when said particular slot is  
14 ready by asserting in said slot one or more found signals that identify  
15 one or more specific ports associated with said one or more  
16 execution resources;

17               (2)   refrain from selecting said particular slot when said particular slot is  
18 not ready by asserting in said slot a lost signal;

19               (3)   track slots that have been selected during said launch cycle; and

20               (4)   direct the selection of no more than said predefined plurality of said  
21 instructions during said launch cycle,

22 wherein an instruction identified as ready for launching is launched on a select instruction  
23 port identified via said set of signals forwarded through said queue, said set of signals  
24 comprising a next available instruction port identifier when an instruction port is available.

1           34.     (Previously Presented) The method of claim 33, further comprising the  
2 step of:

3           communicating said predefined plurality of said instructions from said queue to  
4 said corresponding predefined plurality of ports associated with said one or more  
5 execution resources.

35. (Previously Presented) The method of claim 33, further comprising the step of:

(c) during said launch cycle but after said predefined plurality of said instructions have been selected, propagating a lost signal to remaining slots associated with remaining instructions of said queue to indicate to said remaining slots that their respective remaining instructions have not been selected.

36. (Currently Amended) A system for finding a predefined plurality of instructions, if available, that are ready to be executed in a processor that can launch execution of instructions out of order, comprising:

(a) an instruction reordering mechanism for temporarily storing a plurality of said instructions; and

(b) a plurality of logic elements associated with said instruction reordering mechanism and associated respectively with each of said instructions in said instruction reordering mechanism for causing and preventing launching, when appropriate, of respective instructions, said logic elements configured to propagate a plurality of signals through said logic elements, said plurality of signals responsive to available instruction ports and port information to launch execution of an instruction identified as valid for launching such that an instruction is launched on an instruction port identified via propagation logic forwarded through said logic elements said propagation logic comprising a next available instruction port identifier when an instruction port is available ~~that direct said logic elements to select said predefined plurality of said instructions for launching and de-select any remaining instructions.~~

37. (Previously Presented) The system of claim 36, wherein each of said logic elements is configured to receive said set of signals from a previous logic element, to evaluate said set of signals to determine whether or not to launch a respective instruction, to modify states associated with said set of signals based upon whether or not said respective instruction was launched, and to propagate said set of said signals to a later logic element.

38. (Previously Presented) The system of claim 36, wherein each one of said logic elements is implemented in combinational logic hardware.

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1           39.   (Previously Presented) The system of claim 36, wherein each said logic  
2 element is configured to, after said predefined plurality of said instructions have been  
3 selected, propagate a lost signal to remaining logic elements associated with said  
4 remaining instructions of said instruction reordering mechanism to indicate to said  
5 remaining logic elements that their respective remaining instructions have not been  
6 selected.

1           40.   (Previously Presented) The system of claim 36, further comprising one or  
2 more execution resources having one or more ports to receive data from said predefined  
3 plurality of said instructions.

1           41.   (Previously Presented) The system of claim 40, wherein at least one of said  
2 execution resources is an arithmetic logic unit (ALU).

1           42.   (Previously Presented) The system of claim 40, wherein at least one of said  
2 execution resources is a multiple accumulate unit (MAC).

1           43.   (Previously Presented) The system of claim 40, wherein at least one of said  
2 execution resources is a cache.

1           44.   (Previously Presented) The system of claim 36, wherein said instruction  
2 reordering mechanism is a queue.

1           45.   (Previously Presented) The system of claim 36, further comprising:  
2 an arbitration mechanism configured to assert a start signal to one of said logic  
3 elements to initiate said propagation of said set of signals.

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1           46.    (Currently Amended) A system for finding a predefined plurality of  
2 instructions, if available, that are ready to be executed and that reside in a queue of a  
3 processor that can launch execution of instructions out of order, comprising:  
4           (a)   queue means for storing a plurality of said instructions, said queue means  
5 having a plurality of launch logic means for causing and preventing launching, when  
6 appropriate, of a respective instruction; and  
7           (b)   logic means associated with said queue, said logic means for propagating  
8 a set of signals to successive launch logic means, said set of signals responsive to available  
9 instruction ports and port information to launch execution of an instruction to indicate  
10 both when and which of one or more ports of one or more execution resources are  
11 available for each said instruction and when none of said ports are available, wherein an  
12 instruction identified as valid for launching by said launch logic means is launched on an  
13 instruction port identified via said set of signals forwarded through said launch logic  
14 means and wherein said set of signals includes a next available instruction port identifier  
15 when an instruction port is available.